Axially-doped n^+-p^--n^+ Silicon Nanowire Field Effect Transistors

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Advances in nanomaterial synthesis and self-assembly create a potential route for fabrication of next generation electronic and optical devices with superior performance and functionality.[1,2] Silicon nanowires (SiNWs) are of particular interest as a model system for studying new device phenomena as well as for applications in electronic and sensing circuits.[3,4, 5] However, the relatively immature SiNW synthesis and device integration processes coupled with the limited availability of statistical device data have complicated the interpretation and comparison of the electrical transport properties of SiNWs across different device platforms (e.g., NW vs. planar) and length scales. We present here the results of *n*-channel enhancement-mode MOSFETs fabricated using thermally-oxidized n^+-p^--n^+ SiNWs where electron transport occurs in an inverted p^--channel. These devices show a substantial improvement in electrical properties and reproducibility as compared to those fabricated using uniformly-doped SiNWs, which will facilitate future studies to elucidate the role of scaling on SiNW FET integration and performance.

The SiNWs used in these studies were synthesized by vapor-liquid-solid (VLS) growth from Au catalyst particles using 10% SiH_4 in H_2 as the silicon gas source and phosphine (PH_3) as the n-type dopant. Axially-doped n^+-p^--n^+ SiNWs were grown by changing sequentially the dopant-to-SiH_4 gas flow ratio during SiNW growth (n^+([P:Si]=2×10^{-3}, $\sigma_{4\text{-pt}}\sim3\times10^{-3}\Omega$-cm, L~7µm)-p-(nominally-undoped, $\sigma_{4\text{-pt}}\sim5\times10^{4}\Omega$-cm, L~1µm) -$n^+$([P:Si] = 2×10^{-3}, $\sigma_{4\text{-pt}}\sim3\times10^{-3}\Omega$-cm, L~6µm). Following growth, the Au catalyst particles were removed from the tips of the as-grown SiNWs, and the NWs were cleaned using a modified RCA process prior to dry oxidation at 700°C for 4 hours. Transmission electron microscopy studies showed that the interface between the SiNW core and the ~8 nm thick SiO_2 shell was smooth and uniform without visible tapering along the entire length of the SiNW. A slight change in diameter and surface morphology was observed during the transition between the n^+- and nominally-undoped SiNW segments; the n^+-segments exhibited slightly larger surface roughness that has been observed previously on uniformly n^+-doped SiNWs. These SiNWs were integrated onto a top- and back-gated test structure by electrofludically aligning individual wires between pairs of large area electrodes. Source and drain (S/D) contacts were defined by first removing the SiO_2 shell at the n^+-SiNW ends and then lifting off Ti(100nm)/Au(100nm) metal. Non-self-aligned 3-µm long top gates comprised of Ti(80nm)/ Au(40nm) were then deposited on the SiO_2 gate dielectric over the p^--channel and overlapping part of the n^+-S/D. The n^{++}-Si substrate coated with 100 nm of LPCVD Si_3N_4 was used as a back gate in these structures.

In contrast to uniformly-doped SiNW FETs that operate by depletion of the *p*- or *n*-type NW and have low on-state current I_{on} ~ 10nA@V_{DS} = 1V, the axially-doped SiNW n^+-p^--n^+ FETs (1 µm p^--channel) operate as enhancement mode FETs with a two order of magnitude larger I_{on}~ 3µA@V_{DS} = 1V. Additionally, these SiNW FETs have an on/off ratio I_{on}/I_{off} ~10^7, threshold voltage V_{th} ~1V, subthreshold slope S~0.3V/decade, and transconductance g_m ~1.3µS with negligible hysteresis in the subthreshold characteristics. Measurements using a control sample that probes separately the n^+- and p^--SiNW regions exhibited *n*- and *p*-channel depletion mode characteristics, respectively, which confirmed that radial deposition of *n*-type Si onto the p^--channel region was prevented during growth of the second n^+-SiNW segment. A second control sample was used to show that the n^+-segments decrease the S/D resistance and facilitate the electron transport through an inversion layer. Finally, measurements of more than ten 1-µm long channel SiNW FETs with diameters ranging from 66nm to 83nm showed good uniformity in I_{on} (V_{GS} – V_{th} = 1.5 V and V_{DS} = 1 V) after normalizing device properties for variations in SiNW diameter and gate dielectric thickness. These improved properties and reproducibility promotes the possibility of extracting accurate values of carrier mobility by studying SiNW FETs with varying channel length.

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